DAC8580/81 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the DAC8580/81 Evaluation Module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

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1 EVM Overview

This section gives a general overview of the DAC8580/81 Evaluation Module (EVM) and instructions on setting up and using this evaluation module.

1.1 Features

This EVM features the DAC8580/81 digital-to-analog converter (DAC). It provides a quick and easy way to evaluate the functionality and performance of the high-resolution, serial input DAC. The EVM provides the serial interface header to easily attach to any host microprocessor or TI DSP-based system for communication.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The DC power supply for the digital section (DV_{DD}) of the device under test (DUT) installed on this EVM is selectable between +5 VD and +3.3 VD via the W1 jumper, although the digital pullups are permanently tied to +5 VD. The +5-VD source can come from the J5-1 terminal (if installed) or the J6-10 terminal and is referenced to ground through the J5-2 and J6-5 terminals, respectively.

The DC power supply requirements for the analog section (AV_{DD} and AV_{SS}) of the DUT installed on this EVM is provided by +5 VA that can come from the J5-3 terminal (if installed) or the J6-3 terminal, and -5 VA that can come from J6-4 terminal, respectively. The analog ground is referenced through the J1-2 terminal (if installed) or the J6-6 terminal. The high voltage supply via V_{CC} and V_{SS} is typically ±15 V but can range from ±4.5 V minimum to ±18 V maximum and connect through the J1-1 and J1-3 terminals, respectively (if installed), or through the J6-1 and J6-2 terminals. All of the analog power supplies are referenced to analog ground through the J1-2 and J6-6 terminals.

The V_{CC} supply sources the positive rail of the external output operational amplifier, U2, as well as the REF02 reference source, U3, and the buffer operational amplifier, U8A. The negative rail of U2 is supplied by V_{SS}, although U2 also can be selected to be connected to AGND via W5 jumper. The external operational amplifiers, U2 and U8B, are installed as an option to provide output signal conditioning and for any other output configurations desired.

CAUTION

To avoid potential damage to the EVM board, ensure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The externally generated +5 Vdc, via REF02, or +4.096 Vdc, via REF3040, precision voltage reference is jumper selectable via W4. The reference voltage for the DUT can be chosen between the installed precision reference circuits or user-supplied reference via TP1. The REF02, U3, is the reference source installed from the factory whereas the REF3040, U4, is optional. Because the REF3040 is pin compatible with the REF31xx and REF32xx reference family, the user can choose between these wide varieties of precision references. The REF02 is a 10 ppm/°C with excellent line regulation and stability. The chosen reference source provides the DAC8580/81's voltage output range. An external reference source of up to AV_{DD} can be applied to the reference input via TP1 if other than the onboard reference source is desired.

1.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8580/81 digital-to-analog converter. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TI DSP, or some sort of a signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass-through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8580/81EVM using a custom-built cable.

A TI adapter interface board, the 5-6K Interface Board, is also available to fit and mate with TI's C5000 and C6000 DSP Starter Kit (DSK). This eliminates problems involved in building a custom cable. In addition, this EVM can connect to and interface with an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor. For more details or information regarding the 5-6K Interface Board or the HPA449 platform, call Texas Instruments or send an email to *dataconvapps@list.ti.com*.

The DAC output can be monitored through the J4 header connector. In addition, the DAC output can be connected to the output operational amplifier, U2, by using a jumper across any of the pins 1-2, 3-4, 5-6, or 7-8 of the J4 header terminal. The input signal going into the output operational amplifier, U2, must be configured correctly on the J3 header to achieve the desired output waveform. The output operational amplifier, U2, is configurable through J3, W5, and W15 for any desired waveform characteristic.

Figure 1 a shows a block diagram of the DAC8580/81EVM.

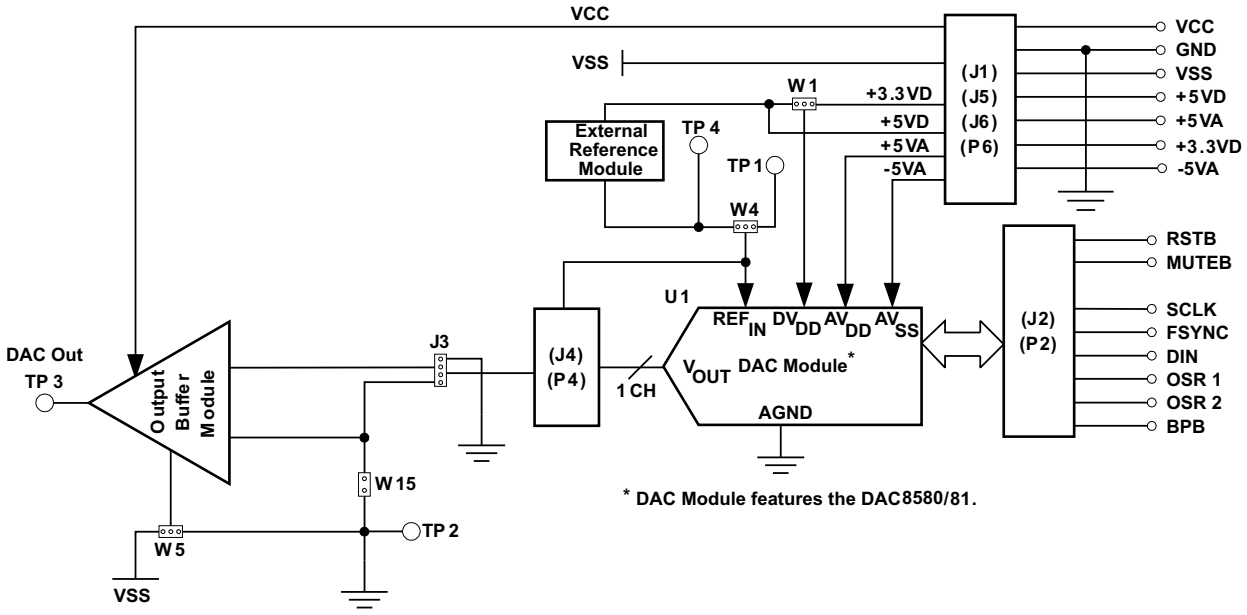


Figure 1. DAC8580/81EVM Block Diagram

2 PCB Design and Performance

This section discusses the layout design of the PCB, describing the physical and mechanical characteristics of the EVM. It shows the resulting performance of the EVM, which can be compared to the device specification listed in the data sheet. The list of components used on the module is also included in this section.

2.1 PCB Layout

The DAC8580/81EVM is designed to demonstrate the performance quality of the installed DAC device under test (DUT), as specified in the data sheet. To take full advantage of the EVM's capabilities, use care during the schematic design phase to properly select the right components and to build the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals, and understanding the component's electrical and mechanical attributes.

The main design concern during the layout process is the optimal placement of components and the proper routing of signals. Place the bypass capacitors as close as possible to the pins, and the analog and digital signals should be properly separated from each other. In the layout process, carefully consider the power and ground planes because of their importance. A solid plane is ideally preferred but because of its greater cost, sometimes a split plane can be used satisfactorily. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contribute to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practices can be seen in Figure 2 through Figure 8.

The DAC8580/81EVM board is constructed on a four-layer printed-circuit board (PCB) using a copper-clad FR-4 laminate material. The PCB has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2000 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2 through Figure 7 show the individual artwork layers.

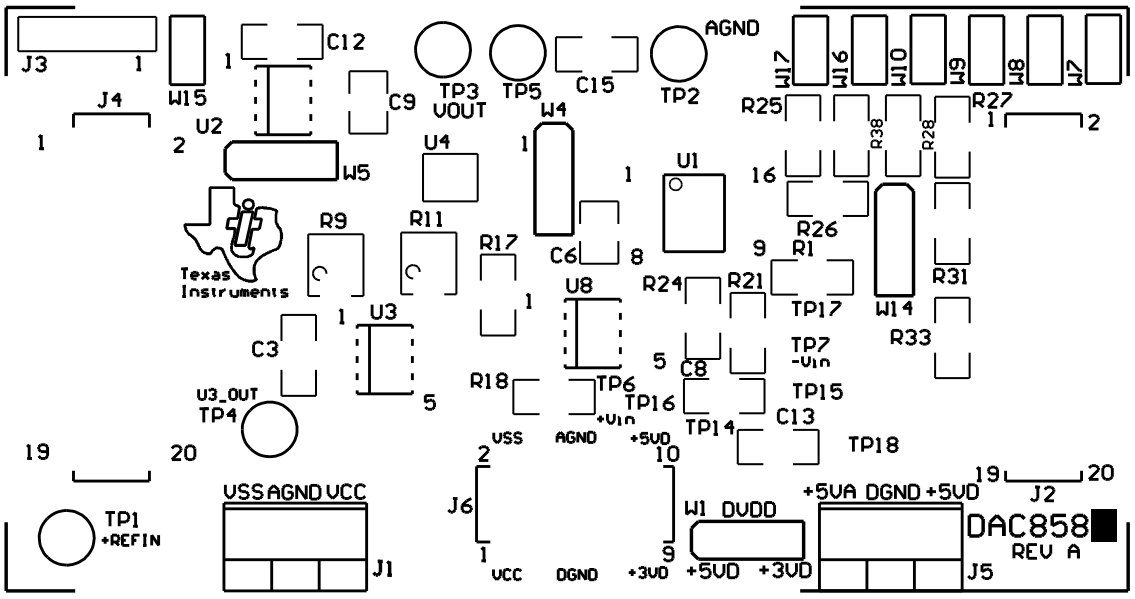


Figure 2. Top Silkscreen

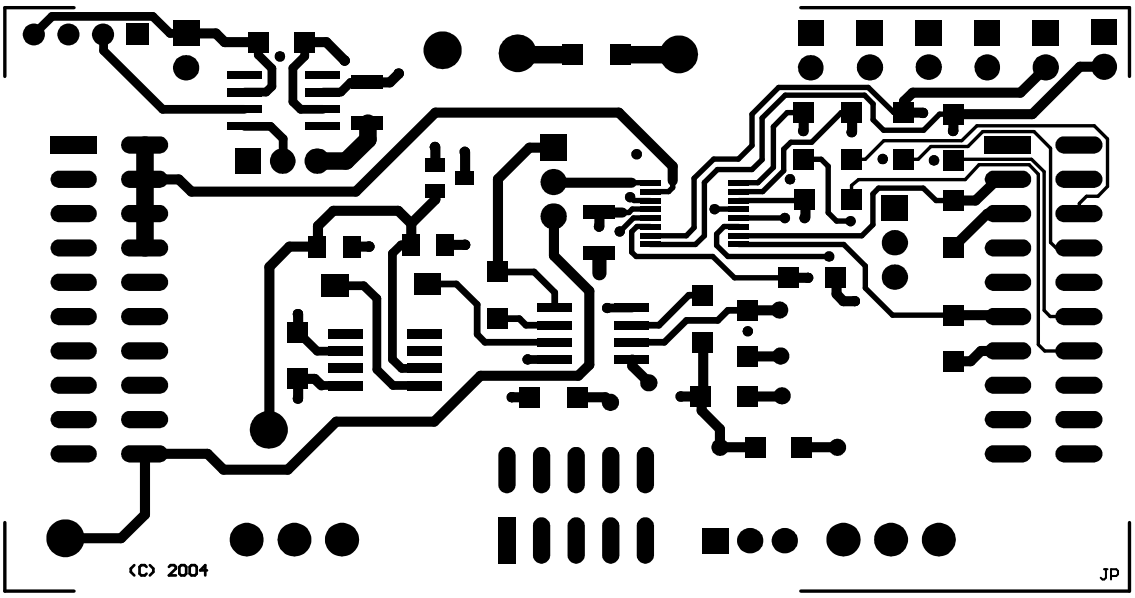


Figure 3. Layer 1 (Top Signal Plane)

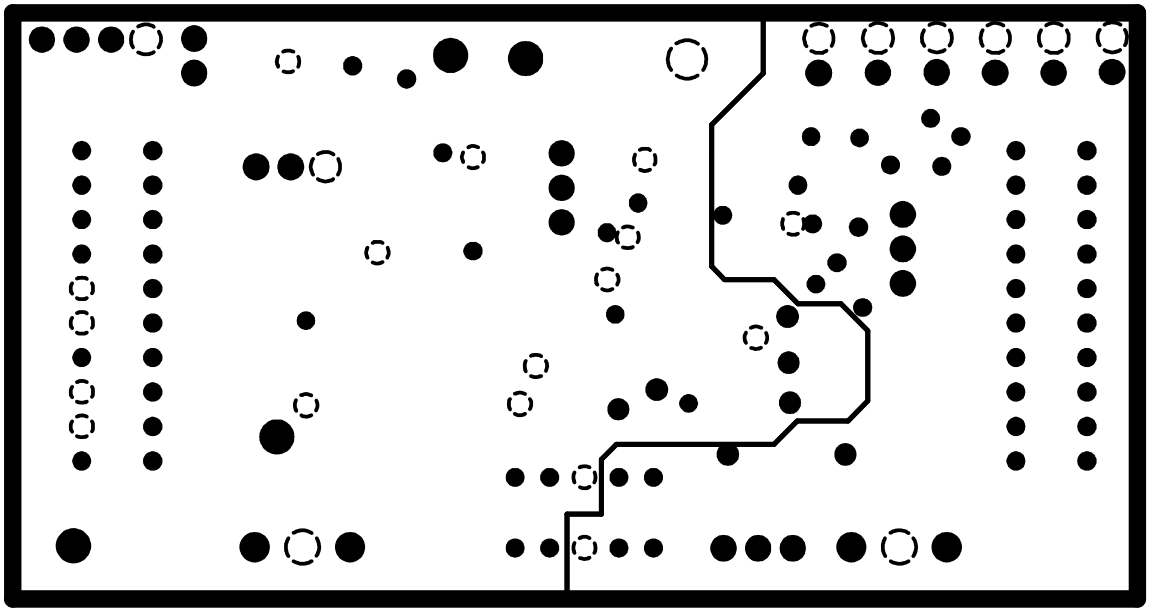


Figure 4. Layer 2 (Ground Plane)

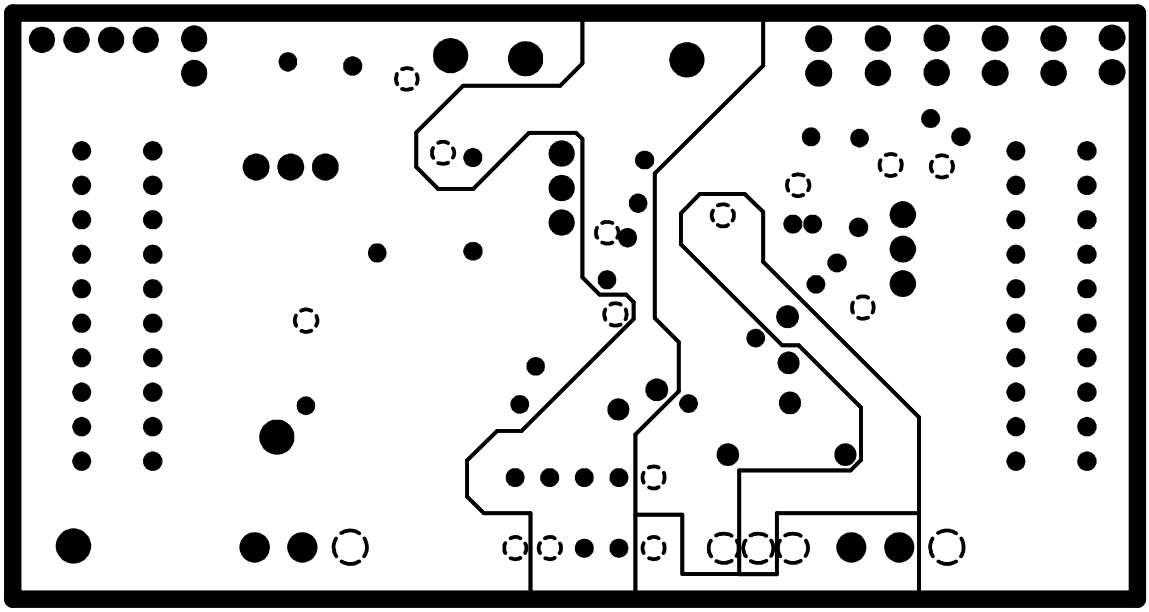


Figure 5. Layer 3 (Power Plane)

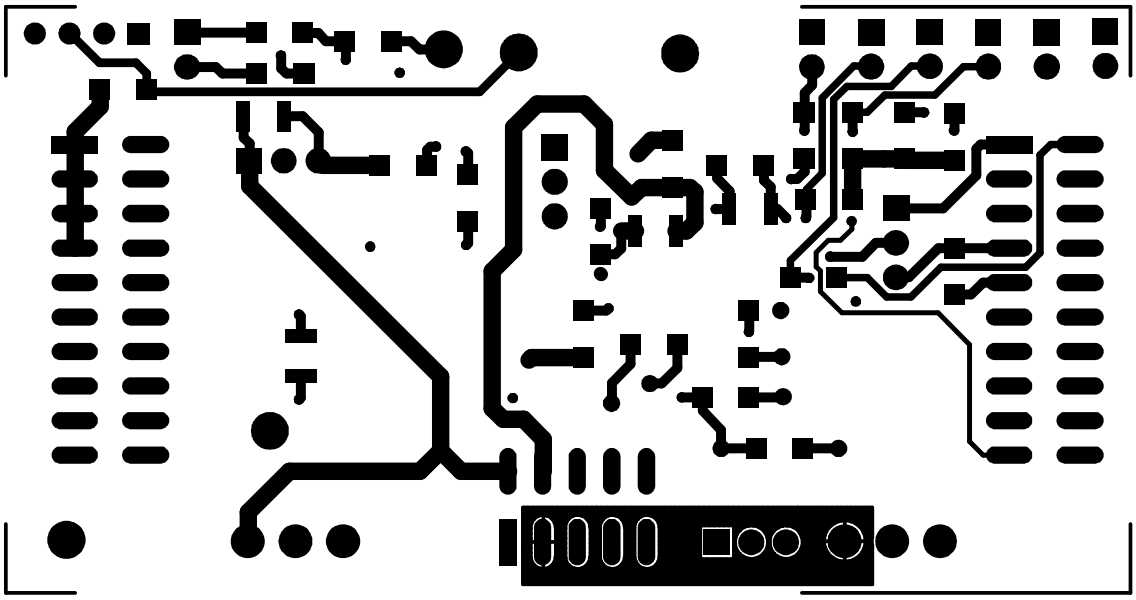


Figure 6. Layer 4 (Bottom Signal Plane)

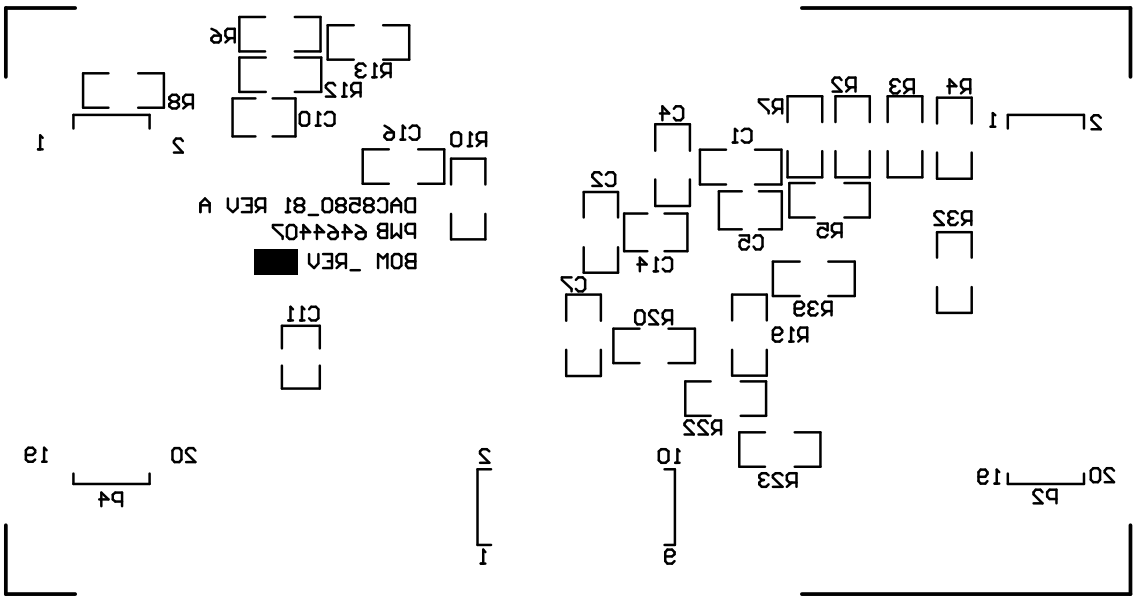


Figure 7. Bottom Silkscreen

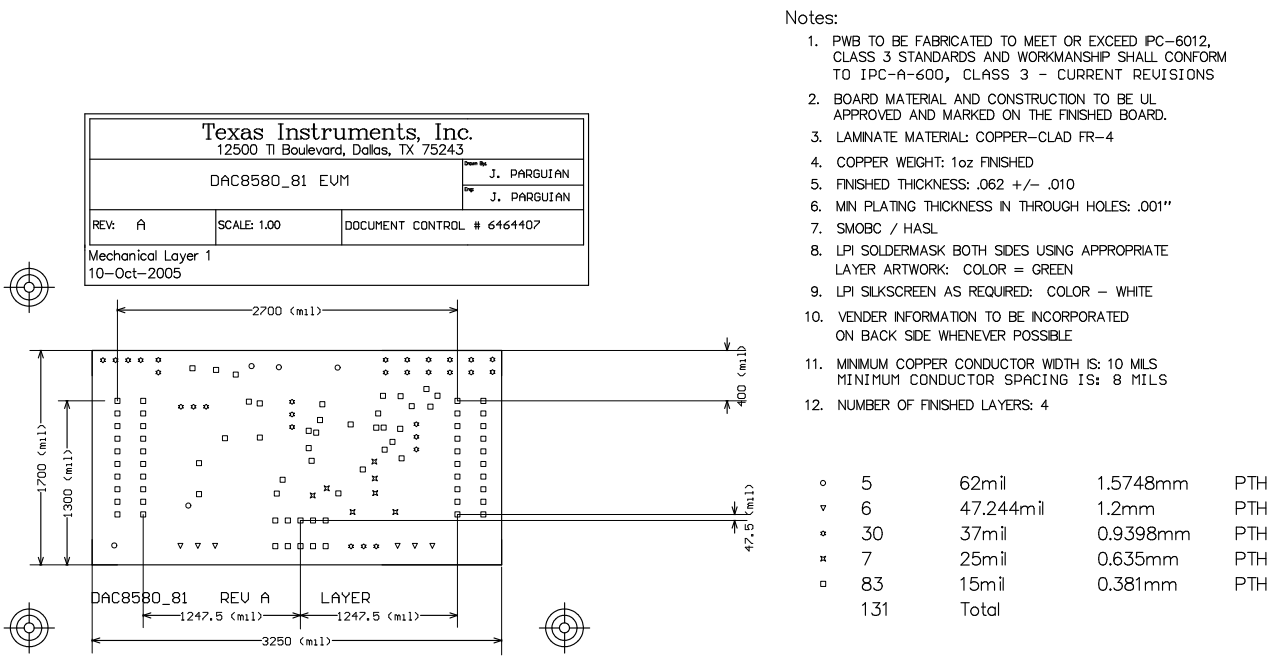


Figure 8. Drill Drawing

2.2 EVM Performance Results

The EVM performance test was achieved using the DAC8580EVM piggy- backed onto the High Interface Board (HIB) for DAC tester, and tested using the Teradyne A580 connected to a personal computer. The EVM board is tested for all codes of the device under test (DUT) and is allowed to settle before the measurement is recorded. This process is repeated for all codes to generate the measurements for INL and DNL results.

The results of the DAC8580/81EVM characterization test are shown in Figure 9 and Figure 10.

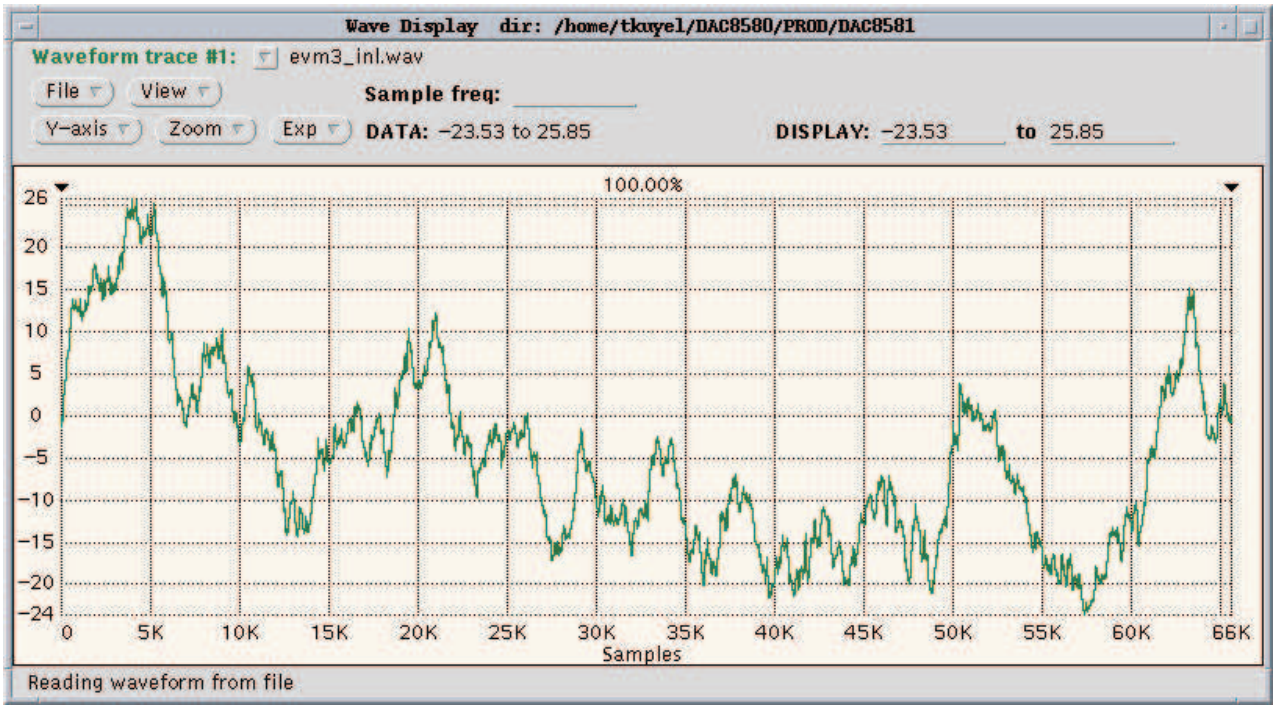


Figure 9. INL Characteristic Plot for the DAC8580

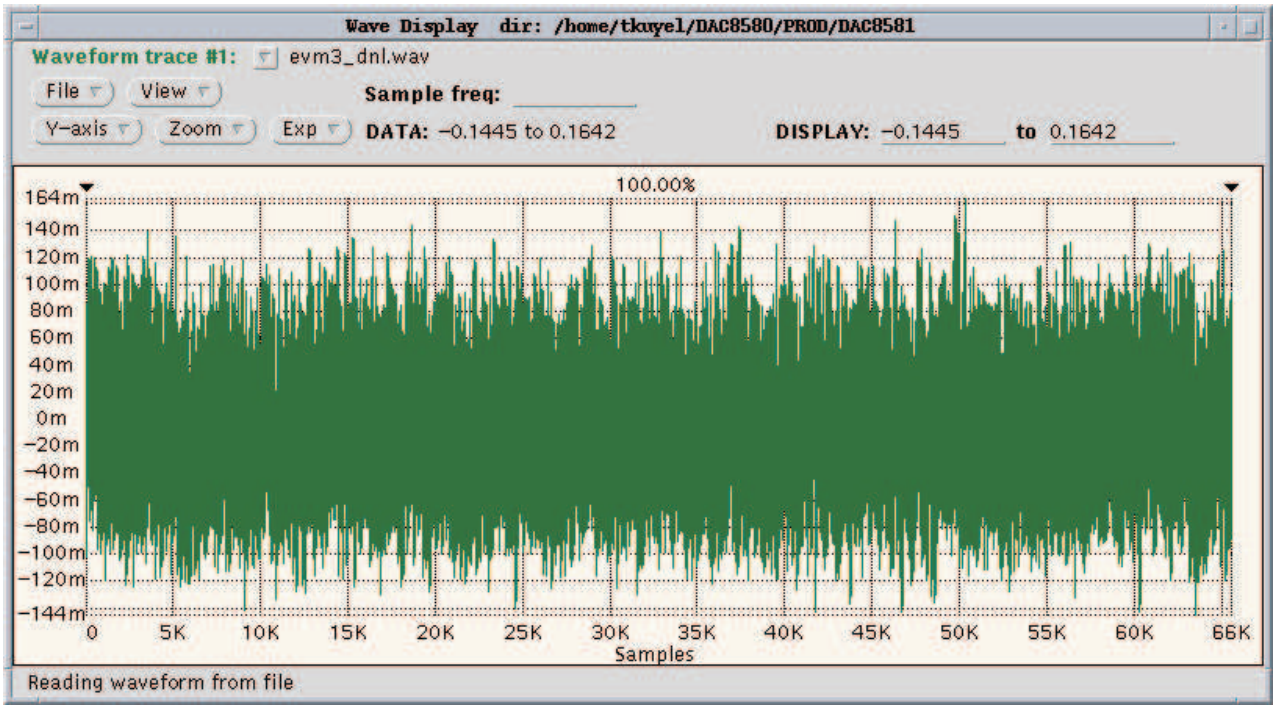


Figure 10. DNL Characteristic Plot for the DAC8580

2.3 Bill of Materials

Table 1 displays the bill of materials.

Table 1. Bill of Materials

Item	Qty	Value	Designators	Description	Vendor	Vendor Part Number
1	10	0 Ω(1)	R17 R25 R26 R27 R28 R31 R32 R33 R38 R39	1/4W 1206 Thick Film Chip Resistor, ±5% Tol(1)	Panasonic	ERJ-8GEY0R00V
2	2	1 µF	C9 C10	Multilayer Ceramic Chip Capacitor, 1206 SMD, 50V, ±15% TC, ±10% Tol	TDK	C3216X7R1H105KT
3	5	0.1 µF	C1 C2 C3 C4 C7	Multilayer Ceramic Chip Capacitor, 1206 SMD, 25V, 0±30ppm/ºC TC, ±10% Tol	TDK	C3216COG1E104KT
4	1	1 nF	C12	Multilayer Ceramic Chip Capacitor, 1206 SMD, 630V, 0±30ppm/ºC TC, ±10% Tol	TDK	C3216COG2J102KT
5	7	2 × 1 × 0.1 TH	W7 W8 W9 W10 W15 W16 W17	Modified 0.025" Square Post Header	Samtec	MTSW-102-08-T-S-295
6	4	3 × 1 × 0.1 TH	W1 W4 W5 W14	Modified 0.025" Square Post Header	Samtec	MTSW-103-08-T-S-295
7	1	5 × 2 × 0.1 SMT	P6	10-PIN Socket Strip(1)	Samtec	SSW-105-22-F-D-VS-K
8	8	10 kΩ	R1 R2 R3 R4 R5 R6 R7 R12	1/8W 1206 Thick Film Chip Resistor, ±1% Tol	Panasonic	ERJ-8ENF1002V
9	1	2 kΩ	R8	1/4W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEYJ202V
10	1	100	R13	1/4W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEYJ101V
11	4	10 µF	C5 C6 C11 C14	Multilayer Ceramic Chip Capacitor, 1210 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3225X7R1E106KT
12	1	20 kΩ	R10	1/8W 1206 Thick Film Chip Resistor, ±1% Tol	Panasonic	ERJ-8ENF2002V
13	2	10 × 2 × 0.1 SMT	P2 P4	20-PIN Socket Strip(1)	Samtec	SSW-110-22-S-D-VS-P
14	1	Bipolar Op Amp	U8	8-SOP(D) Dual, High Precision, Low Noise Operational Amplifier	Texas Instruments	OPA2227UA
15	1	100 kΩ POT	R11	5T Potentiometer, 4mm SMD, Cermet	Bourns	3214W-104E
16	1	20 kΩ POT	R9	5T Potentiometer, 4mm SMD, Cermet	Bourns	3214W-203E
17	1	16-Bit DAC	***U1**	High-speed, Low-noise, Voltage Output DAC(1)	Texas Instruments	DAC8580IPW DAC858IPW
18	2	3 × 1 × 0.138 TH	**J1 J5**	3-Pin Terminal Block(1)	On-Shore Tech.	ED555/3DS
19	1	Difet Op Amp	U2	8-SOP(D) Precision High-speed Operational Amplifier	Texas Instruments	OPA627AU
20	1	5V Voltage Reference	U3	Precision Voltage Reference	Texas Instruments	REF02AU
21	4	1 × 1 × 0.061D TH	TP1 TP2 TP3 TP4 TP5	Turret Terminal Pin	Mill-Max	2348-2-00-01-00-00-07-0
22	2	10 × 2 × 0.1 SMT	J2 J4	20-PIN Terminal Strip	Samtec	TSM-110-01-S-DV-M
23	1	5 × 2 × 0.1 SMT	J6	10-PIN Terminal Strip	Samtec	TSM-105-01-T-DV
24	1	470 pF	C15	Capacitor 50V Ceramic Chip 1206 SMD	TDK	C3216X7R1E471KT
25	1	4 × 1 × 0.1 TH	J3	Modified 0.025" Square Post Header	Samtec	MTSW-104-08-T-S-295
26	1	4.096 V Voltage Reference	U4	SOT23-3, 4.096 V Precision Voltage Reference, 50ppm/°C(1)	Texas Instrument	REF3040AIDBZT
27	10	To be determined	**C8 C13 C16 R18 R19 R20 R21 R22 R23 R24**	**DO NOT INSTALL**		
28	7	Test point pins	**TP6 TP7 TP14 TP15 TP16 TP17 TP18**	**DO NOT INSTALL**		

(1) P2, P4, and P6 parts are not shown in the schematic diagram. All the P-designated parts are installed in the bottom side of the PCB opposite the J-designated counterpart. For example, J2 is installed on the top side whereas P2 is installed in the bottom side opposite of J2. **The following parts: J1, J5, R31, R32, and R33 and items 27 and 28 are NOT installed. C16 and U4 are optional; U4 can be substituted for U3 for external reference source. The DUT installed, U1, for the EVM is either a DAC8580 or DAC8581 device. For the DAC8581, the following parts are not installed in addition to the preceding listing: R1, R2, R3, R4, R25, R28, R38, R39, W7, W8, W9 W10, and W17. Jumper wires are installed in lieu of W7, W8, W9, and W10.**

3 EVM Operation

This section covers in detail the EVM operation to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a host processor.

See the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide for more information about the DAC's serial interface and other related topics.

The EVM board is factory-tested and configured to operate in the bipolar output mode.

3.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described in Table 2 to operate in bipolar ±5-V output operation as measured from TP5. The default jumper settings below are shown in Figure 11 and Figure 12 for each respective EVM.

Table 2. DAC8580/81EVM Factory Default Jumper Setting

DAC8580/81EVM Jumper Default Configuration		
Reference	**Jumper Position**	**Function**
W1	2-3	DV_{DD} is powered at +3.3 VD.
W4	1-2	DAC reference is sourced externally from U3.
W5	1-2	Negative supply rail of U2 operational amplifier is sourced by V_{SS}.
W7	CLOSE	OSR1 is tied low, configured for 2x oversampling rate. This is hardwired to DGND for the DAC8581EVM.
W8	CLOSE	OSR2 is tied low, configured for 2x oversampling rate. This is hardwired to DGND for the DAC8581EVM.
W9	CLOSE	RSTB is tied low so the DAC is configured for conventional operation. Digital filter is disconnected. This is hardwired to DGND for the DAC8581EVM.
W10	CLOSE	BPB is tied low so the DAC is configured for conventional operation. Digital filter is disconnected. This is hardwired to DGND for the DAC8581EVM.
W14	1-2	The CS signal is routed to FSYNC to synchronize the data word.
W15	CLOSE	Output operational amplifier is configured for a gain of 2.
W16	OPEN	MUTEB/CLR is high so that the DAC8580/DAC8581 output is not set to midscale (~0V).
W17	CLOSE (For DAC8580EVM)	For the DAC8580EVM, this jumper must be connected to digital ground reference for proper operation.
	OPEN (For DAC8581EVM)	For the DAC8581EVM, this jumper must be connected to DV_{DD} for proper operation; therefore, the jumper is not installed
J3	2-3	DAC output is tied to the non-inverting input of the output operational amplifier.
J4	1-2	DAC V_{OUT} is routed to the J3 jumper.
J6	5-6	AGND and DGND are tied together.

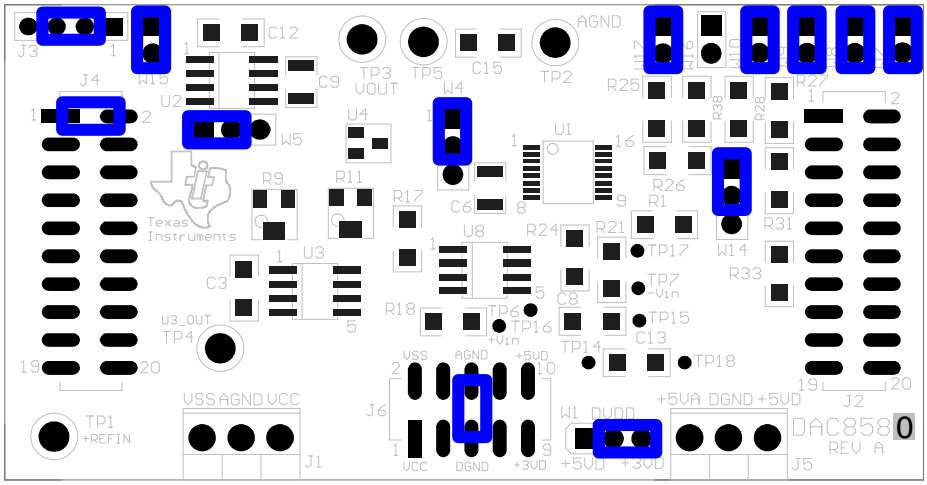


Figure 11. DAC8580EVM Default Jumper Setting

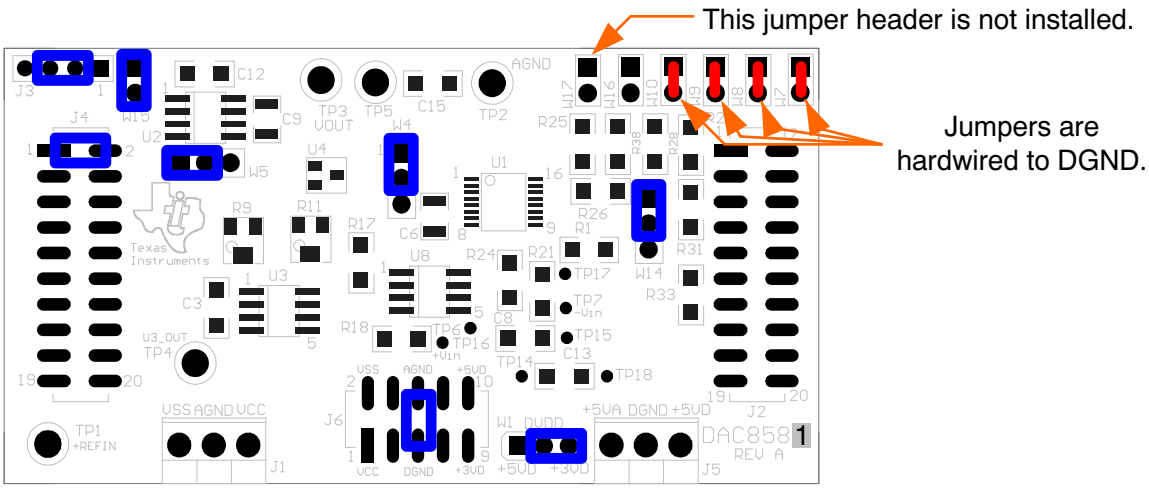


Figure 12. DAC8581EVM Default Jumper Setting

3.2 Host Processor Interface

The host processor basically drives the DAC; therefore, the DAC's proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 and P2 pass-through header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

A TI Interface Board is also available for a specific TI DSP Starter Kit as well as an MSP430-based microprocessor as mentioned in Section 1 of this manual. Using the interface board foregoes the task of building customized cables and allows easy configuration of a simple evaluation system.

This DAC EVM interfaces with any host processor capable of handling serial communication protocols or the popular TI DSP. For more information regarding the serial interface of the particular DAC installed, see the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide.

3.3 The Output Operational Amplifier

The EVM includes an optional signal-conditioning circuit for the DAC output through an external operational amplifier, U2. The output operational amplifier is set to unity gain configuration by default. Nevertheless, the raw output of the DAC can be probed through the even pins of the output terminal, J4.

The inverting input of U2 can be tied to the gain resistor, R12 (via W15) or the DAC output (by shorting pins 3 and 4 of the J3 header) or to any voltage source through J3-4.

The following sections describe the different configurations of the output amplifier, U2. This operational amplifier can be used to serve as buffer to unload the DAC and also different signal conditioning and amplification purposes desired.

This buffering circuit may present some slight distortion because of the feedback resistor and capacitor. If this is the case, users can easily configure the feedback circuit to closely match the desired wave shape by simply removing R6 and C12 and replacing it with the proper values. Users can also eliminate R6 and C12 altogether and solder a 0-Ω resistor in replacement of R6, if desired.

3.3.1 Unity Gain Output

Table 3 shows the jumper setting for the unity gain configuration of the DAC output buffer in unipolar or bipolar mode.

Table 3. Unity Gain Output Jumper Settings

Reference	Jumper Position		Function
	Unipolar	Bipolar	
J3	2-3	2-3	Routes the DAC output to the non-inverting terminal of the output operational amplifier, U2.
W15	OPEN	OPEN	Disconnect the inverting input of the operational amplifier, U2, from gain resistor, R12.
W5	2-3	1-2	Negative rail of operational amplifier is tied to AGND or powered by V_{SS}.

3.3.2 Output Gain of Two

Table 4 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 4. Gain of Two Output Jumper Settings

Reference	Jumper Position		Function
	Unipolar	Bipolar	
J3	2-3	2-3	Routes the DAC output to the non-inverting terminal of the operational amplifier, U2.
W15	CLOSED	CLOSED	Inverting input of the output operational amplifier, U2, is connected to gain resistor, R12, to set for a gain of 2.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for bipolar supply mode or ties it to AGND for unipolar supply mode.

3.3.3 Output Gain of Five With DAC V_{OUT} Inverted

Table 5 shows the proper jumper settings of the EVM to achieve a gain of five with the output of the DAC inverted.

Table 5. Jumper Settings for a Gain of Five With Inverted Output

Reference	Jumper Position		Function
	Unipolar	Bipolar	
J3	1-2 & 3-4	1-2 & 3-4	Output of DAC is inverted with a gain of five. Watch for clipping due to operational amplifier headroom issue.
W15	OPEN	OPEN	Disconnect the inverting input of operational amplifier, U2, from the gain resistor, R12.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for bipolar supply mode, or ties it to AGND for unipolar supply mode.

The inverted output gain of five is shown in Figure 13, where the reference voltage is set to +2.5 V. The raw output of the DAC is ±2.5 V as measured from TP5 as shown by channel 2, and the inverted DAC output is ±12.5 V as measured from TP3 as shown by channel 1.

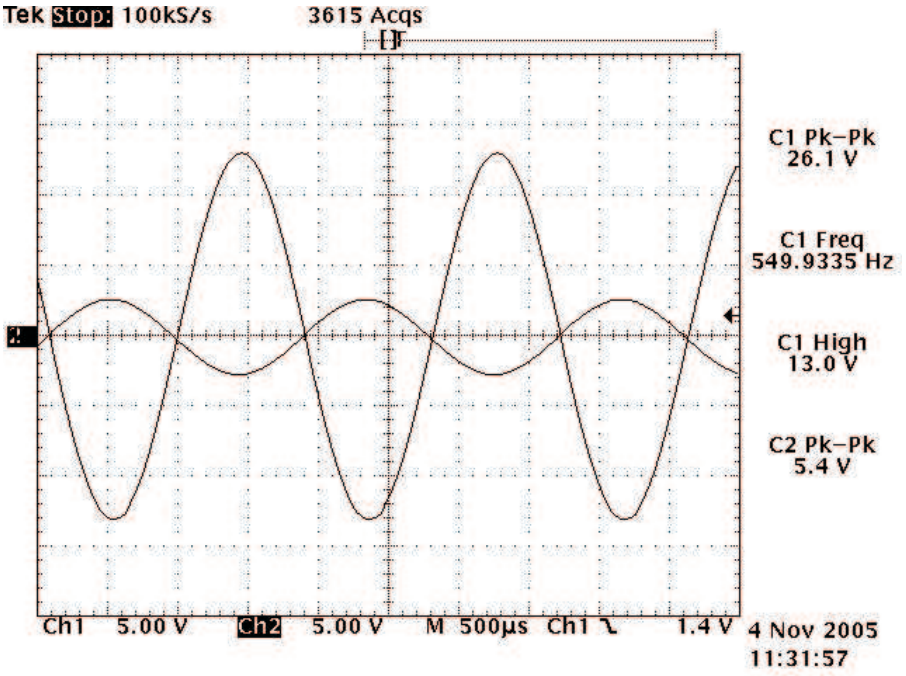


Figure 13. DAC Output Waveform

3.4 Jumper Setting

Table 6 shows the function of each specific jumper setting of the EVM.

Table 6. Jumper Setting Function

Reference	Jumper Setting	Function
W1	1 3 	Routes the +5-V power supply to DAC DV_{DD} pin.
	1 3 	Disconnect the power supply to DAC DV_{DD} pin.
	1 3 	Routes the +3.3-V power supply to DAC DV_{DD} pin.
W4	1 3 	Routes the onboard reference to the V_{REF} pin of the DAC.
	1 3 	Disconnect the onboard reference supply to the V_{REF} pin of the DAC.
	1 3 	Routes the user supplied external reference via TP1 to the V_{REF} pin of the DAC.
W5	1 3 	Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
	1 3 	Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.

Table 6. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
W7		Disconnect the OSR1 input pin of the DAC from ground and ensure a high state configuration for the OSR1 pin. This is hardwired to ground for the DAC8581EVM.
		Connect the OSR1 input pin of the DAC to ground. This is hardwired to ground for the DAC8581EVM.
W8		Disconnect the OSR2 input pin of the DAC8580 from ground and ensure a high-state configuration for the OSR2 pin. This is hardwired to ground for the DAC8581EVM.
		Connect the OSR2 input pin of the DAC to ground. This is hardwired to ground for the DAC8581EVM.
W9		Disconnect the RSTB input pin of the DAC8580 from ground and ensure a high-state configuration for the RSTB pin. This is hardwired to ground for the DAC8581EVM.
		Connect the RSTB input pin of the DAC to ground. This is hardwired to ground for the DAC8581EVM.
W10		Disconnect the BPB input pin of the DAC8580 from ground and ensure a high-state configuration for the BPB pin. This is hardwired to ground for the DAC8581EVM.
		Connect the BPB input pin of the DAC to ground. This is hardwired to ground for the DAC8581EVM.
W14		The FSYNC pin of the DAC is driven by CS pin from J2-1 terminal.
		The FSYNC pin of the DAC is driven by FSX pin from J2-7 terminal.
W15		Disconnect the inverting input pin of operational amplifier, U2, from the gain resistor, R12.
		Connect the inverting input pin of operational amplifier, U2, to the gain resistor, R12 for 2x output gain.
W16		Disconnect the MUTEB/CLR pin of the DAC8580/DAC8581 from AGND and configure it for normal operation.
		Connect the MUTEB/CLR pin of the DAC8580/DAC8581 to AGND and set the DAC output to midscale (~0V).
W17		Should not be installed for proper operation of the DAC8581EVM.
		Should be installed for proper operation of the DAC8580EVM.
J3		The non-inverting input of U2 is tied to AGND.
		DAC V_{OUT} is routed to the non-inverting input of U2.
		DAC V_{OUT} is routed to the inverting input of U2.
		DAC V_{OUT} is routed to the inverting input of U2 and the non-inverting input of U2 is tied to AGND.
Legend:  Indicates the corresponding pins that are shorted or closed.		

3.5 Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, identify the manual by its title and literature number. Updated documents can also be obtained through the TI Web site at www.ti.com.

Data Sheets	Literature Number
DAC8580	SLAS458
DAC8581	SLAS481
OPA227/2227	SBOS110
REF3040	SBVS032
REF02	SBVS003

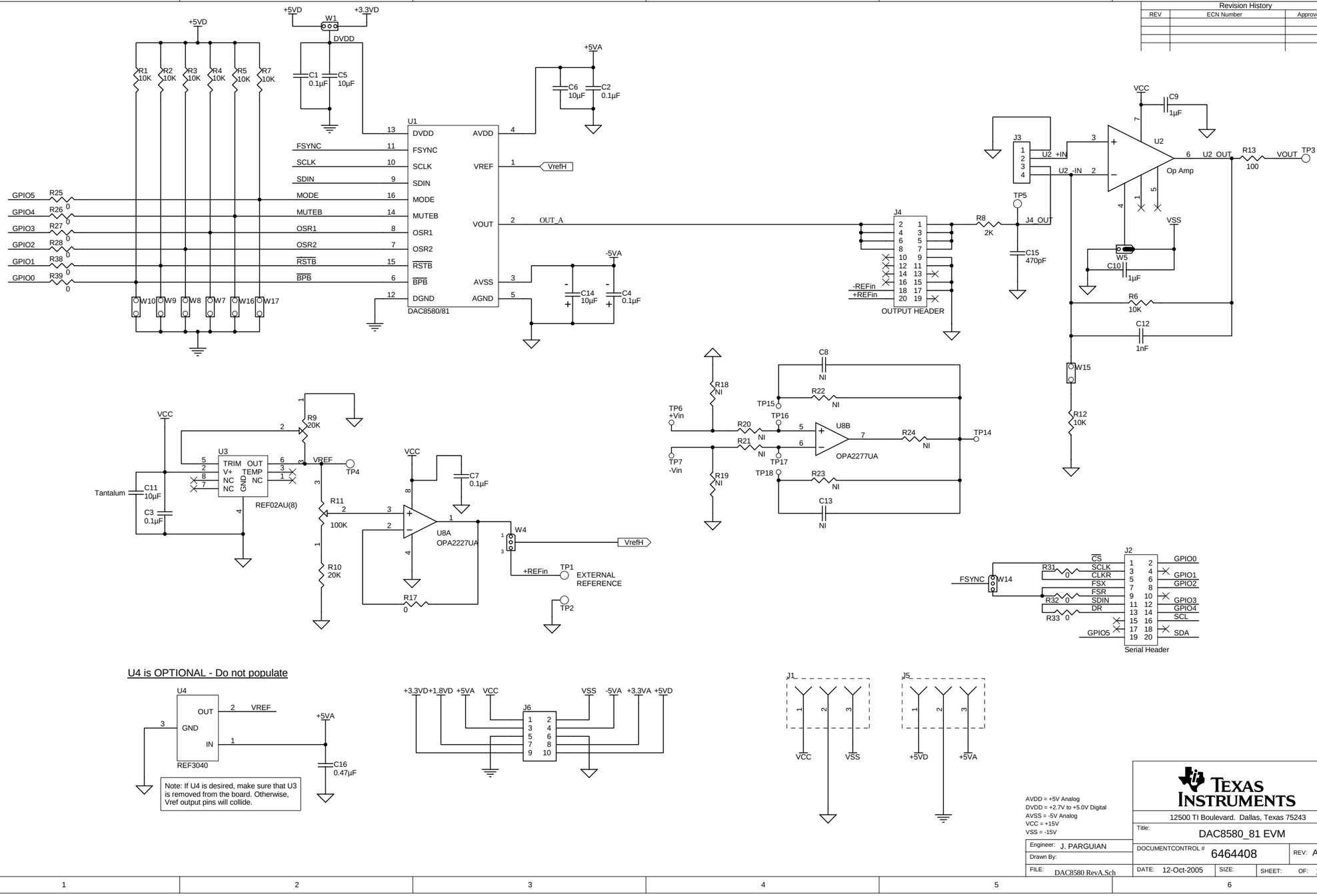
3.6 Questions About This or Other Data Converter EVMs?

If you have questions about this or other Texas Instruments data converter evaluation modules, send an e-mail to the Data Converter Application Team at *dataconvapps@list.ti.com*. Include in the subject heading the name of the product in which you are interested.

3.7 Schematic

The schematic appears on the following page.

Revision History		
REV	ECN Number	Approved



AVDD = +5V Analog
DVDD = +2.7V to +5.0V Digital
AVSS = -5V Analog
VCC = +15V
VSS = -15V

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title:	DAC8580_81 EVM		
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6464408	REV: A	
Drawn By:			
FILE: DAC8580 RevA.Sch	DATE: 12-Oct-2005	SIZE:	SHEET: OF: 1

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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EVM WARNINGS AND RESTRICTIONS (continued)

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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